CLAIMS

We claim:

1. A method for programming a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein the method for programming comprises:

applying electrical ground to the source;

applying a first voltage having a first polarity to the drain;

applying a second voltage of the first polarity to the control gate; and

applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate,

wherein the first, second and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers generated by a secondary impact ionization mechanism, the hot carriers being injected into the at least one charge storage dielectric layer from a drain side of the memory cell.

2. The method of claim 1, wherein absolute values of each of the first, second and third voltages are 5 V or less.

3. The method of claim 1, wherein a difference of absolute values of any two voltages of the first, second and third voltages is 1.5 V or less.

4. The method of claim 1, wherein an effective gate-to-substrate voltage applied by the second and third voltages is at least 4 V.

5. The method of claim 4, wherein absolute values of each of the second third voltages are 5 V or less.

6. The method of claim 1, wherein the charge storage dielectric layer is positioned between two oxide layers.

7. The method of claim 1, wherein the charge storage dielectric layer comprises nitride.

8. A method for erasing a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein the method for erasing comprises:

applying electrical ground to the source;

McDONNELL BOEHNEN
HULBERT & BERGHOFF
300 SOUTH WACKER DRIVE
CHICAGO, ILLINOIS 60606
TELEPHONE (312) 913-0001

applying a first voltage having a first polarity to the drain;

applying a second voltage having a second polarity opposite to the first polarity to the control gate; and

applying a third voltage of the second polarity to the semiconductor substrate,

wherein the first, second and third voltages cooperatively effect erasing of the memory cell as a result of injection of hot carriers generated by substrate-enhanced-band-to-band-tunneling induced hot-carrier-injection, the hot carriers being injected into the at least one charge storage dielectric layer from a drain side of the memory cell.

9. The method of claim 8, wherein absolute values of each of the first, second and third voltages are 5 V or less.

10. The method of claim 9 wherein a difference of absolute values of any two voltages of the first, second and third voltages is 1.5 V or less.

11. A method for reading, in a reverse direction, a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein the memory cell is programmed by applying electrical ground to the source, applying a first voltage having a first polarity to the drain, applying a second voltage of the first

McDONNELL BOEHNEN
HULBERT & BERGHOFF
300 SOUTH WACKER DRIVE
CHICAGO, ILLINOIS 60606
TELEPHONE (312) 913-0001

polarity to the control gate, and applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate, and wherein the method of reading comprises:

applying electrical ground to the drain and the semiconductor substrate;

applying a first voltage having the first polarity to the source;

applying a second voltage having the first polarity to the gate electrode; and

sensing whether or not current is flowing from the drain towards the source.

12. A memory circuit comprising:

an array of single bit nonvolatile memory cells, each of the memory cells comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer;

peripheral circuitry, the peripheral circuitry coupled with the memory cell such that programming and erasing of each memory cell is effected using voltages having absolute values of 5 V or less.

13. The memory circuit of claim 12, wherein the peripheral circuitry comprises circuitry for generating an on-chip voltage, having an absolute value of 5V or less.

14. A memory circuit, comprising:

an array of single bit nonvolatile memory cells organized in columns, wherein each of the memory cells comprises a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a gate electrode and a dielectric stack, the gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein:

adjacent memory cells in each column of the memory circuit have one of their sources and their drains in common;

the sources of the memory cells in each column of the memory circuit are coupled with the same bitline, the bitline running parallel with the column;

the drains of the memory cells in each column of the memory circuit are coupled with a respective wordline, the wordline running perpendicular to the column; and

the gates of the memory cells in each column of the memory circuit are coupled with a respective program line, the program line running perpendicular to the column.

15. A method for programming a memory cell in the memory circuit of claim 14, the method comprising:

applying electrical ground to a first bitline;

applying a first voltage having a first polarity to a wordline;

applying a second voltage of the first polarity to a program line;

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HULBERT & BERGHOFF
300 SOUTH WACKER DRIVE
CHICAGO, ILLINOIS 60606
TELEPHONE (312) 913-0001

applying a third voltage, having a second polarity opposite to the first polarity to the semiconductor substrate; and

applying a fourth voltage of the first polarity to all other bitlines of the memory circuit.

16. The method of claim 15, wherein absolute values of each of the first, second and third voltages are 5 V or less, and an absolute value of the fourth voltage is 2 V or less.